AMENDMENT TO THE SPECIFICATION

Please amend the specification as follows:

[0005] In a more complex class of cascaded CAM systems, the priorities of individual entries in the search database are programmable, for example, to simplify the insertion and deletion of database entries having intermediate priorities. In such programmable-priority CAM systems, each constituent CAM device having a key-matching entry outputs both the match address and a corresponding priority value[[[,]]] and wherein resolution of multiple match conditions involves a comparison of priority values output by competing CAM devices to determine a priority winner.

[0019] The CAM system 200 responds to a host-supplied search instruction and search key by carrying out a multi-phase search operation. In the first phase, referred to herein as the primary search phase, the individual CAM devices 201 concurrently search their local (i.e., internally maintained) databases for key-matching entries and produce corresponding local match results. Each local match result includes a match address and a corresponding priority-match (PM) value. The PM value itself includes a match flag that indicates whether a key-matching entry was detected within the local database and a priority number that corresponds to the match address and reflects the priority of the key-matching entry relative to other entries within the local database. In one embodiment, the match flag is a single-bit active low signal and the priority numbers are multi-bit entities that indicate priorities in inverse proportion to their numeric value. Thus, a match indication is indicated by a logic low match flag, and priority numbers having lower numeric values indicate a higher priority than priority numbers having higher numeric values (other priority ordering schemes and/or opposite match flag logic states may be used in alternative embodiments). Using this scheme, the match flag may be viewed as a most-significant bit of a PM value so that any PM value having a low match flag (i.e., match detected) is ensured to have a lower numeric value, and therefore a higher priority, than any PM value having a high match flag (i.e., no match detected). If multiple key-matching

entries are detected within a given CAM device 201 (i.e., a multiple match condition), priority resolution logic within the CAM device produces a match address and PM value that correspond to the key-matching entry associated with ~~the highest-priority priority number~~priority number having the highest priority.

[0023] After a match-indicating final priority winner is resolved by the top-tier CAM device $201_{1,1}$, the final phase of the search operation is initiated. In the final phase, one or more ~~enable~~ output enable operations are executed to enable the CAM device that produced the final priority winner to output its local match address onto the result bus (i.e., source the HPM). In one embodiment, referred to herein as a sequential-enable embodiment, each CAM device 201 in the hierarchy waits to receive an active-low match enable signal at an output enable input (OE) before executing an output enable operation. Match enable signals are issued in sequence from one tier of CAM devices 201 to the next, progressing downward through the hierarchy of CAM devices 201 until the CAM device that produced the final priority winner is reached. Upon receiving a match enable signal, a CAM device 201 executes an output enable signal by either (1) outputting its match address onto the result bus (i.e., sourcing the HPM) if the local PM value was the local priority winner or (2) outputting a match enable signal to the child CAM device that provided the local priority winner. As shown in Figure 3, the output enable input of the top-tier CAM device $201_{1,1}$ is tied low so that, as soon as the final priority winner is resolved, the top tier CAM device $201_{1,1}$ is enabled to execute an output enable operation and thus either sources the HPM (if the local PM value of the top tier CAM device $201_{1,1}$ was the final priority winner) or outputs a match enable signal to a child CAM device (i.e., one

of mid-tier CAM devices $201_{2,1}$-$201_{2,N}$) via one of match enable outputs ME_1-ME_N according to the final priority winner. If the top-tier CAM device $201_{1,1}$ did not source the final priority winner, then the mid-tier CAM device that provided the final priority winner will receive a match enable signal at its output enable input and perform an output enable operation in response. That is, the mid-tier CAM device will either source the HPM or output a match enable signal to one of the bottom-tier CAM devices in its family according to the local priority winner previously determined within the mid-tier CAM device. If the mid-tier CAM device did not produce the local priority winner, then the bottom-tier CAM device that provided the local priority winner to the mid-tier CAM device will receive a match enable signal at its output enable input and thus be enabled to perform an output enable operation. Because the bottom tier CAM device received no valid PM values from lower tier CAM devices, the bottom tier CAM device is the local priority winner (i.e., in the comparison performed by the bottom tier CAM device) and therefore sources the HPM.

[0034] Reflecting on the timing diagram of Figure 7, it should be noted that, while two pipelined search operations are illustrated, each stage of the pipeline (including internal search stages used to generate local PM values and match addresses) may be consumed by a separate search operation (i.e., the pipeline is fully loaded) so that a continuous stream of search operations are carried out within the CAM system 300, with a new result being output onto the result bus during each successive pair of clock cycles. Also, while two clock cycles are shown for many of the pipeline stages, such operations may alternatively be consumed in more or fewer clock cycles, or in fractions of a clock cycle as in Figure 5. Further, while pipelined search operations have ~~has~~ been described in the context of CAM system 300 of Figure 6, pipelined search operations may

similarly be executed for the CAM system 200 of Figure 3.

[0044] The configuration circuit 405 is also coupled to the controller 441 and supplies the controller 441 with the above-described configuration information [[[~~that~~]]] to control how long the controller 441 waits relative to a clock signal edge or other timing reference (e.g., a signal from the core CAM that a search operation has been begun or is completed) before asserting the compare-strobe signal. Thus, if the configuration circuit indicates that the CAM device is a bottom-tier CAM device, the control circuit may accordingly issue the compare strobe signal immediately after the local PM value becomes valid. Conversely, if the configuration circuit indicates that the CAM device is a mid-tier or top-tier CAM device, the controller 441 may issue the compare-strobe signal after a delay interval that corresponds to the amount of time required for child CAM devices to supply valid PM values at the priority-match inputs, times that will differ for each [[[~~of~~]]] tier of the hierarchical CAM system.